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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,622	10/27/2000	Jyh-Ming Jong	P4928/06145.003001	4922

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	3

DATE MAILED: 11/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,622	JONG ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it is too short. Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claim 8 is objected to because of the following informalities: in line 17, after detected inserts a --.--. A period is needed at the end of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Tateishi U.S. Patent No 5,790,613.

As per claims 1, 8 and 9, Tateishi discloses an apparatus for detecting a noise error of a signal comprising: an upper comparator is the same as the claimed (high comparator) (see figs.5, 8-10, 13-15 element 8U1 and col.6, lines 29-30, 45-55) that references a high voltage limit with

the signal and generates an output; a low comparator (see figs.5, 8-10, 13-15 element 8L1 and col.6, lines 29-30, 45-55) that references a low voltage limit with the signal and generates an output; and a circuit (see figs.5, 8-10, 13-15 element 88 and col.6, lines 25-67) that processes the high comparator output and the low comparator output, wherein the circuit generates a trigger is considered as the claimed (alarm) if a noise error is detected (see col.7, lines 49-50 and col.8, lines 46-47 and col.10, lines 40-45).

As per claim 2, the apparatus of Tateishi does include a high-to-low sub-circuit that detects a noise error during a rising signal transition and a low-to-high sub-circuit that detects a noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20) .

As per claim 3, the apparatus of Tateishi does include: a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59).

As per claim 4, the apparatus of Tateishi does include a differential amplifier (see fig.5 element 820).

As per claim 5, the apparatus of Tateishi inherently includes sense amplifier.

As per claim 6, the apparatus of Tateishi inherently includes high voltage limit and the low voltage limit is 300 mV.

As per claims 7 and 13, the apparatus of Tateishi discloses an apparatus for detecting a noise error of a signal comprising: an upper comparator is the same as the claimed (high

comparator) (see figs.5, 8-10, 13-15 element 8U1 and col.6, lines 29-30, 45-55) that references a high voltage limit with the signal and generates an output; a low comparator (see figs.5, 8-10, 13-15 element 8L1 and col.6, lines 29-30, 45-55) that references a low voltage limit with the signal and generates an output, wherein the difference between the high voltage limit and the low voltage limit is 300 mV; a high-to-low sub-circuit that detects a noise error during a rising signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the high-to-low sub-circuit comprises, a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59); a low-to-high sub-circuit that detects a noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the low-to-high sub-circuit comprises: a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59) wherein either sub-circuit generates an alarm if a noise error is detected a trigger is considered as the claimed (alarm) if a noise error is detected (see col.7, lines 49-50 and col.8, lines 46-47 and col.10, lines 40-45).

As per claim 10, the apparatus of Tateishi inherently includes high voltage limit and the low voltage limit is 300 mV.

As per claim 11, the apparatus of Tateishi does include wherein the low signal voltage is compared with the low voltage limit by a low-to-high sub-circuit that detects the noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-

46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the low-to-high sub-circuit comprises, a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59).

As per claim 12, the apparatus of Tateishi does include wherein the high signal voltage is compared with 2 the high voltage limit by a high-to-low sub-circuit that detects the noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the low-to-high sub-circuit comprises, a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kondoh U.S. Patent No 6,404,976 B1 teaches a Viss signal detection circuit.

Van Leeuwen et al U.S. Patent No 5,539,340 teaches a circuit for detecting pulses and video recorder.

Mores et al U.S. Patent No 6,111,443 teaches an accelerated switching by selection of various threshold levels.

Cho U.S. patent No 4,924,483 teaches a track counting circuit for use in an optical disk driver.

Ohta U.S. patent No 5,909,414 teaches an optical information recording.

Norton U.S. patent No 5,455,720 teaches an offset and gain error.

Draxelmayr U.S. patent No 6,404,242 B2 teaches a comparator circuit.

Yang et al U.S. Patent No 6,400,658 B1 teaches a DVD-RAM disk.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is (703) 308-9573. The examiner can normally be reached on Monday-Thursday from 8:00 AM - 5:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour , can be reached on (703) 306-3034. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Emmanuel Bayard

Primary Examiner

November 24, 2003